Application Note
IXZ631DF18N50
13.56 MHz Class E

By
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Introduction

The IXZ631DF18N50 ultra-fast RF power module combines a IXRFD631 driver and IXZ318N50L MOSFET into one package, decreasing both the footprint size and the parts count on a PCB. In addition, there is up to 25% cost savings over using separate packages.

The following is an evaluation circuit for the IXZ631DF18N50 in a low-order class E topology that produces 600 watts CW at a frequency of 13.56 MHz. Efficiency is greater than or equal to 88% at 600 W output into a 50 Ω load.

This circuit is for component evaluation and demonstration purposes only. It is not a plan for a finished product, but rather a general starting point for industrial, commercial, and scientific amplifier applications.

Figure 1 is the schematic.

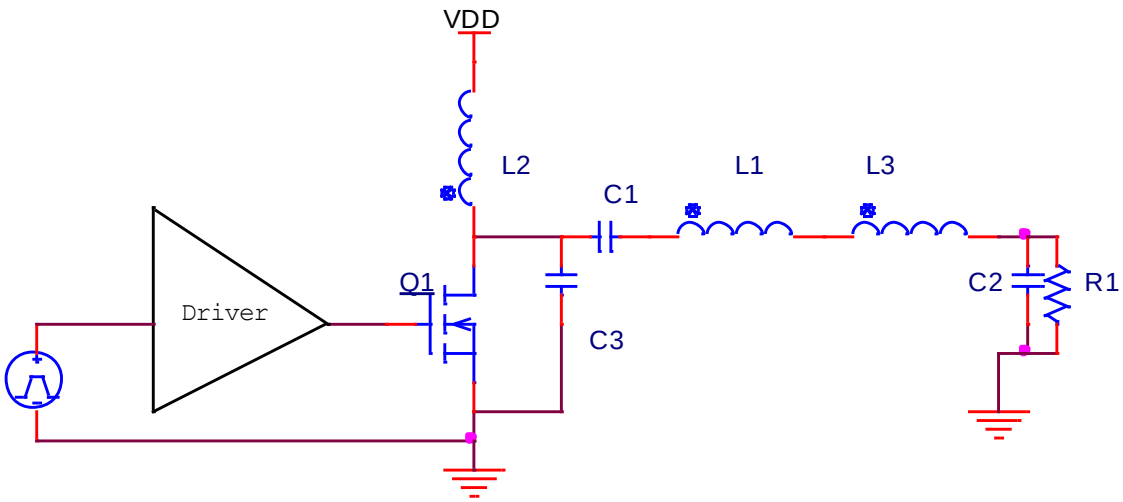


Figure 1

The components are as follows:

C1 is the series capacitance of the resonant tank

C3 represents the C_{OSS} of the MOSFET and any added shunt capacitance

L1 is the series tank inductance

L3 is the L network inductance

C2 is part of the matching L network

L2 is the choke inductor (10 µH)

R1 is the output load (50 Ω)

The generator specifications are as follows:

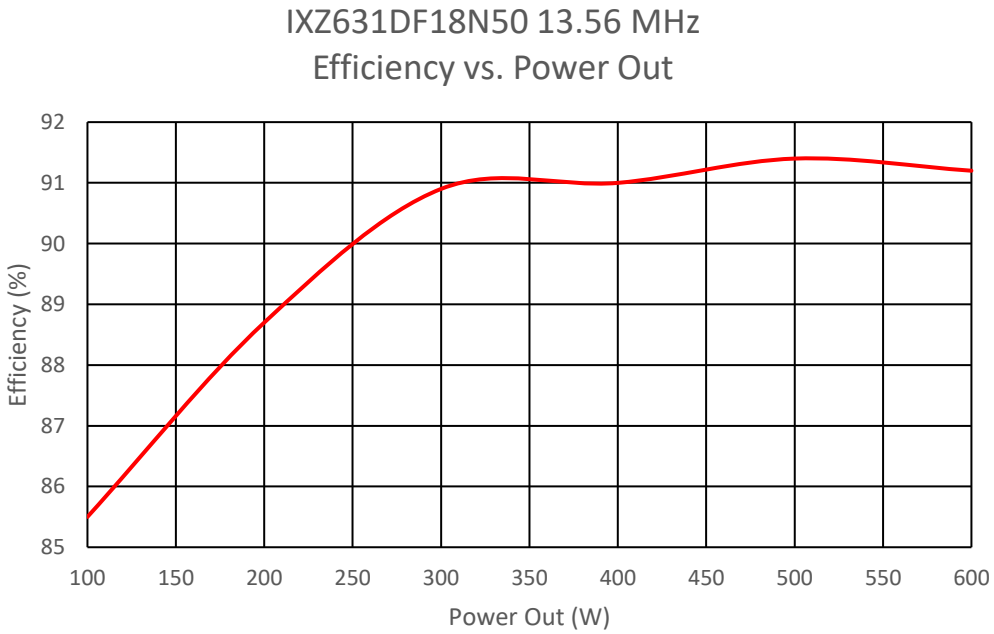
QL = 2

RL = 8 Ω

Vdd = 155 V

Data

P_{OUT} (W)	V_{IN} (V)	I (A)	P_{IN} (W)	Eff. (%)	Vp Drain (V)	DCLL Ω
100	67	1.75	117	85.5	174	38.3
200	94	2.4	226	88.7	252	39.2
300	113	2.92	330	90.9	312	38.7
400	130	3.38	439	91	368	38.5
500	144	3.8	547	91.4	418	37.9
600	157	4.19	658	91.2	468	37.5



Description

The Class E topology is a switch-mode power amplifier that achieves high efficiency through the design of a resonant output network, where the transient response prevents high current and high voltage across the active device at the same time. In theory, the generator is capable of 100% efficiency. The only power wasted is across the R_{dsON} and the ESR in the passive components of the tank circuit. This is achieved by the series circuit C1, L1, and C3 as shown in figure 1. As you will see, C1 and L1 are not resonant at the design frequency. This is not a tuned circuit; rather, it is part of a “flywheel” circuit to ensure the correct voltage waveform is generated on the drain of the MOSFET [1]. This voltage waveform should have a duty cycle of 50%.

Design

There are three values to take into consideration when determining if the MOSFET is capable of 13.56 MHz in the design of your class E generator. These values are QL, RL of the tank circuit, and the C_{OSS} of the MOSFET to be used as the switch. The QL is the chosen Q of the tank circuit. This is left up to the designer, but one thing to note is that the higher the value of Q, the lower the usable frequency will be in this configuration. The Q can be no less than 1.7879[2] in value. The next value to consider is the RL of the tank circuit. This is the impedance of the tank circuit for the output load. When determining this, I have always chosen a value of at least 10 times the MOSFET's R_{dsON}. The third value is the C_{OSS} of the device that will be used for the main switch. This capacitance is part of the tank circuit, and if this value is too large, the component will not be very efficient as a class E generator. This is due to the capacitance not being fully discharged before the MOSFET is switched on again. The larger the capacitance, the longer the discharge period will be. The following formula is used to determine the Shunt capacitance. The C_{OSS} of the device you choose for your design needs to be equal or less than the value in formula 1.

Shunt Capacitance

Formula 1 $$(1+\left(\frac{1}{QL}\right))/(6.3*2*\pi*f*RL)$$ [2]

An RL of 8 Ω was chosen for this circuit, which is 20 times larger than the R_{dsON} of the 18N50 MOSFET and a Q of 2. Using these values in formula 1 yields a total shunt capacitance of 350 pF. This value represents both the C_{OSS} of the MOSFET and any other added capacitance needed. The IXZ318N50 MOSFET has a C_{OSS} of about 250 pF at 150 V on the drain. This value is estimated from the capacitance chart on the data sheet. I subtract the C_{OSS} value from the calculated shunt capacitance to get the value of the added capacitance; in this case it is 100 pF and can be adjusted later when tuning the circuit.

The next value to determine is the tank series capacitance. The formula is:

Series Capacitance

Formula 2 $$(1+\left(\frac{1}{QL}\right))/(2*\pi*f*QL*RL)$$ [2]

The value of the series tank capacitance is 1100 pF. We will start with this value and adjust it as we begin to tune the generator; the adjustment is needed due to our inability to create an inductor with an exact value.

The next value is the tank inductance, L1. The formula is:

Resonant Tank Inductance

Formula 3 $$L1=\frac{Ql*RL}{2*\pi*f}$$ [2]

The value of the tank inductor is 188 nH. This will not be the final value of L1 since we will be combining a matching L network inductance with this value.

We now have the values needed for a high-power class E generator with an output load of 8 Ω. In this evaluation, the output load is 50 Ω, so we must transform the 8 Ω impedance of the resonant tank circuit into the 50 Ω output resistance. For this we will use a matching L-network consisting of a series inductance and a parallel capacitance. The network will match the RL of the tank circuit to the output load resistance and work as a low pass filter. The L-network is based on a technique known as *series-parallel transformations*: For any series combination of a resistance R_S and a reactance X_S, there is a parallel combination of R_P and X_P that appears to the same as the voltage applied across the series combination. [3] The RL is 8 Ω and the output load in this case is 50 Ω.

To calculate the values needed for the L-network the following formulas were used:

Formula 4 $$Q = \sqrt{(\frac{Rp}{Rs} - 1)}$$ [3, 5]

Formula 5 $$Rp = Rs * (Q^2 + 1) \; and \; Rs = \frac{Rp}{Q^2+1}$$ [3, 5]

Formula 6 $$Xs = Q * Rs \;\; and \; Xp = \frac{Rp}{Q}$$ [3, 5]

Using the first formula we determine the Q of the L-network with Rp = 50 Ω and Rs = 8 Ω. When these values are used in formula 4 we get a Q of 2.29. Now using formula 6 we will determine Xp and Xs. Xp will be 21.83 Ω and Xs will be 18.32 Ω. To determine the component values for the inductance and capacitance use the following formulas:

Formula 7 $$L = \frac{Xs}{2*\pi*f}$$ [5]

Formula 8 $$C = \frac{1}{2*\pi*f*Xp}$$ [5]

The calculated value for the inductance is 215 nH and the value for the capacitance is 540 pF. The network inductance is now added to the calculated tank inductance; since the two inductors will be in series, the total inductance is 403 nH. This is the value of L1 in the circuit shown at the beginning of the report. The calculated values will differ slightly from the actual component values used. In this design, I will be using a T200-6 toroid core, and the closest value that I can achieve to 403 nH is 360 nH. This will be 6 turns on this core (one more turn adds 100 nH, too much). To compensate for this, we will adjust the series capacitance by adding small amounts of capacitance when I tune the tank circuit. These formulas do not consider the losses from ESR.

The final component of the class E amplifier is the RF choke inductor. At minimum, this inductor should have an inductive reactance of 30 times the RL. The ideal RF choke should look like an open circuit to the DC power supply at the frequency of operation [9, 10, 11, and 12] and provide constant current to the tank circuit. The minimum value of the inductor was 3 µH, but having a higher value of inductance will not affect the operation of the circuit. When the 3 µH was tested in the circuit, a noticeable decrease in power and efficiency was observed. This was resolved with a RF choke of 10 µH; no improvements or decreases of circuit operations were noticed with larger values.

The following is a list of the actual component values used for testing the 13.56 MHz class E generator tuned output circuit as shown in figure 1. All capacitors are 2500 V ATC

porcelain. These capacitors can be substituted with Dielectric Labs equivalents. Note that the drain peak voltage can approach 500 V, and due to the resonant tank action, the tank L/C common point can approach QL x Vp, or 1 kVp. [1, 2, and 13]

Shunt Capacitance = 101 pF (one 56 pF, one 27 pF, and one 18 pF)

Series Capacitance = 1186 pF (two 560 pF ATC100E561JW5000X and two 33 pF ATC)

Total Tank Inductance = 400 nH (6 turns #12 AWG on a T200-6 iron powder core for a value of 360 nH)

Choke inductance = 10 µH (40 turns #20 AWG on a T106-2 core)

Output Capacitance = 430 pF (three 100pf ATC100C101JW2500X, two 56 pF ATC100C560JW2500X, and one 18 pF)

For more information on the final tuning adjustments that might be needed, please refer to references 1, 2, 4, and 13.

The following is a brief description of the IXRFD631 driver section of the class E amplifier.

The driver translates the adjustable-width TTL level signal GATE_DRIVE_PULSE to a 15 Vp and 10 Ap pulse capable of driving the MOSFETs 2000 pF gate. Although the V_{gs} threshold is in the range of 2.5 V to 5 V, the gate is driven to 15 Vp to ensure device saturation and minimal $I^2 * R_{dsON}$ losses. [13]

Driving a MOSFET gate in Class E operation with sub-10 ns rise and fall times can require a large amount of power. The calculated drive power requirement for the 18N50A with 2000 pF and 15 Vp gate voltage swing is 6W using $P = Ciss*V^2*f$. In addition, the driver has internal timing and anti-cross-conduct circuitry that dissipates additional power. The total input drive power is on the order of 31.5 W (15 V, 2.1 A). [13]

The following description of the driver section is from the IXRFD631 data sheet and remains true for the driver/MOSFET module for proper operation.

The driver is a CMOS high-speed high-current gate driver specifically designed to drive MOSFETs in Class D and E HF RF applications at up to 30 MHz, as well as other applications requiring ultrafast rise and fall times or short minimum pulse widths. The driver can source and sink 20 A of peak current while producing voltage rise and fall times of less than 4 ns and minimum pulse widths of 8 nS. The input of the driver is compatible with TTL or CMOS and is fully immune to latch-up over the entire operating range. Designed with small internal delays, cross conduction/current shoot-through is virtually eliminated in the driver.

The circuit's very high switching speed and high frequency operation requires one to pay close attention to several important issues with respect to circuit design. The three key elements are circuit loop inductance, V_{CC} bypassing and grounding.

Circuit Loop Inductance

The V_{CC} to V_{CC} ground current path defines the loop which will generate the inductive term. This loop must be kept as short as possible. The output lead must be no further than

0.375 inches (9.5mm) from the gate of the MOSFET. Furthermore, the output ground leads must provide a balanced symmetric coplanar ground return for optimum operation.

Vcc Bypassing

For the circuit to turn the MOSFET on properly, the driver must be able to draw up to 20A of current from the V_{CC} power supply in 2-6ns. This means that there must be very low impedance between the driver and the power supply. The most common method of achieving this low impedance is to bypass the power supply at the driver with a capacitance value that is at least two orders of magnitude larger than the load capacitance. Usually, this is achieved by placing two or three different types of bypassing capacitors, with complementary impedance curves, very close to the driver itself. (These capacitors should be carefully selected, low inductance, low resistance, and high-pulse current-service capacitors). Care should be taken to keep the lengths of the leads between these bypass capacitors and the driver to an absolute minimum. The bypassing should be comprised of several values of chip capacitors symmetrically placed on either side of the IC. Recommended values are 0.1 µF, 0.01 µF, 0.001 µF, 0.47 µF chips, and at least two 4.7 µF tantalums.

Grounding

For the design to turn the load off properly, the driver must be able to drain this 20 A of current into an adequate grounding system. There are three paths for returning current that need to be considered: Path #1 is between the driver and its load. Path #2 is between the driver and its power supply. Path #3 is between the driver and whatever logic is driving it. All three of these paths should be as low in resistance and inductance as possible, and thus as short as practical.

Operating Conditions

NOTE: The module package must be properly heat sunk. Water cooling is preferred but a heat sink with a very low thermal resistance and forced air cooling will be adequate for intermittent use. A heat sink is not supplied.

Topology: Class E

Supply voltage: Vdd = 160 V (this is also the drain-to-source voltage, Vds)

Input power requirements: 5V TTL signal at 13.56 MHz, pulse width = 26 nS

Output Load: 50 Ω ±2 Ω capable of dissipating 1000 W

Equipment used at IXYSRF for testing:

Bird model 4421 RF power meter with model 4024 power sensor (to measure output power)

Xantrek XFR150-18 DC power supply, 0-155 V, 0-18 A

Bird Termaline Coaxial Resistor, 1000 W, 50 Ω

Tektronix TDS 3032B 300 MHz Oscilloscope

PMK PHVS662-L High Voltage Probe

Vizatek DC power supply (used for the driver section)

Fluke 87V DMM digital

Tektronix AFG3252 Function Generator

Operation Instructions:

1. Insure the circuit board is mounted to a heat sink with a small thermal impedance.
2. Check 50 Ω RF load resistor. Ensure that the load is capable of dissipating 1000 W and measures 50 Ω ±2%.
3. Connect Vizatek DC power supply or any 15 V, 4 A power supply and set to 15 V to the VCC input connector.
4. Connect Xantrek power supply, set to 0 V to the VDD connector.
5. Connect a 1000 W (minimum) power meter that is capable of reading both forward and reflected power to the RF output conn2.
6. Connect the 50 Ω 1000 W RF load to the output of the 1000 W power meter.
7. Connect the function generator to conn1. Set the generator to 13.56 MHz, 26 nS pulse width. The output of the generator must be set to 5 V.
8. Attach a high-voltage probe across the drain to source of the component.
9. Turn on the 15 V supply and the function generator.
10. Monitor the 15 V input current. This current should remain below 3.0 A and above 1.9 A.
11. Turn on the high-voltage power supply and slowly increase the voltage until there is 600 W of output power. Monitor the drain-to-source voltage. If the waveform becomes unstable, decrease the power supply to 0 V and increase the pulse width of the generator to 27 ns. Repeat this step if necessary.
12. Measure the peak voltage of the drain to source. This voltage should be between 440 V and 490 V. See figure 2. If this voltage is too high, add 5 pF to 10 pF to the shunt capacitance C12, C13. If this voltage is too low, remove 5 pF to 10 pF from the shunt capacitance.
13. To calculate the efficiency, use Pout / Pin, **Pin = Vdd * Id**.

The results on the lab test 600 W Version are as follows:

Vdd = 157 V

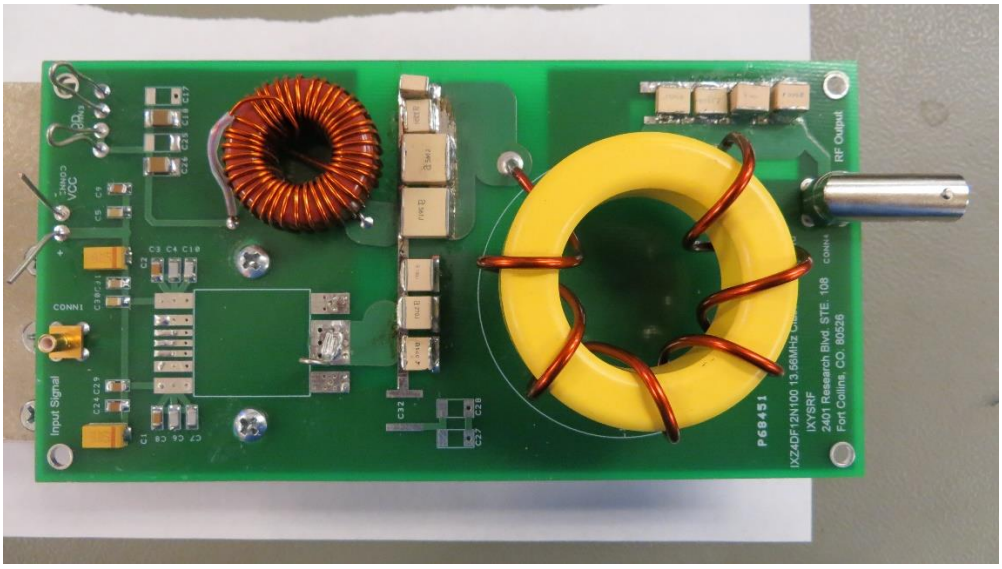
I_{DC} = 4.19 A

Pout = 600 W

Vpeak = 468 V

Eff. = 91.2%

DCLL = 37.5 Ω



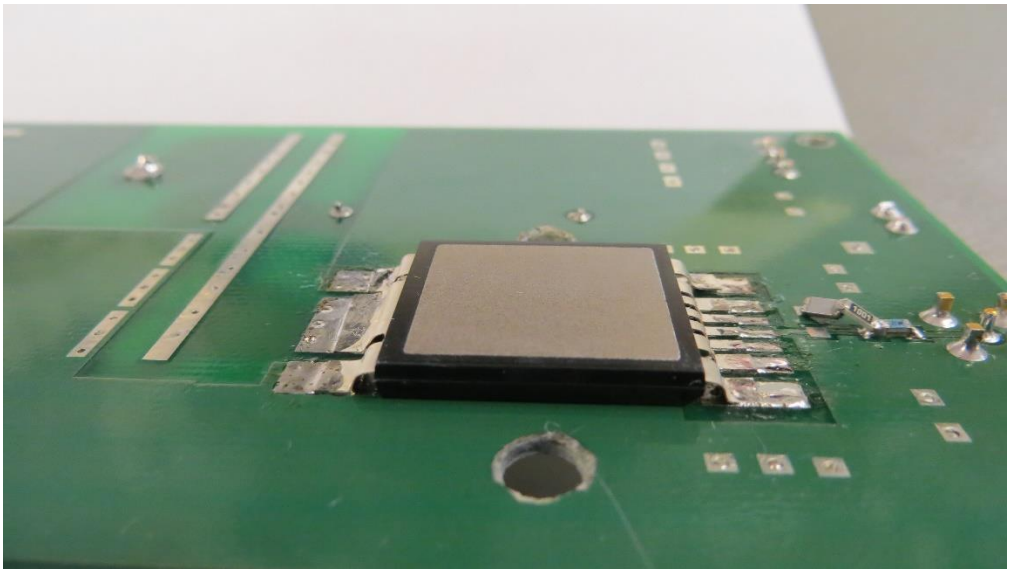
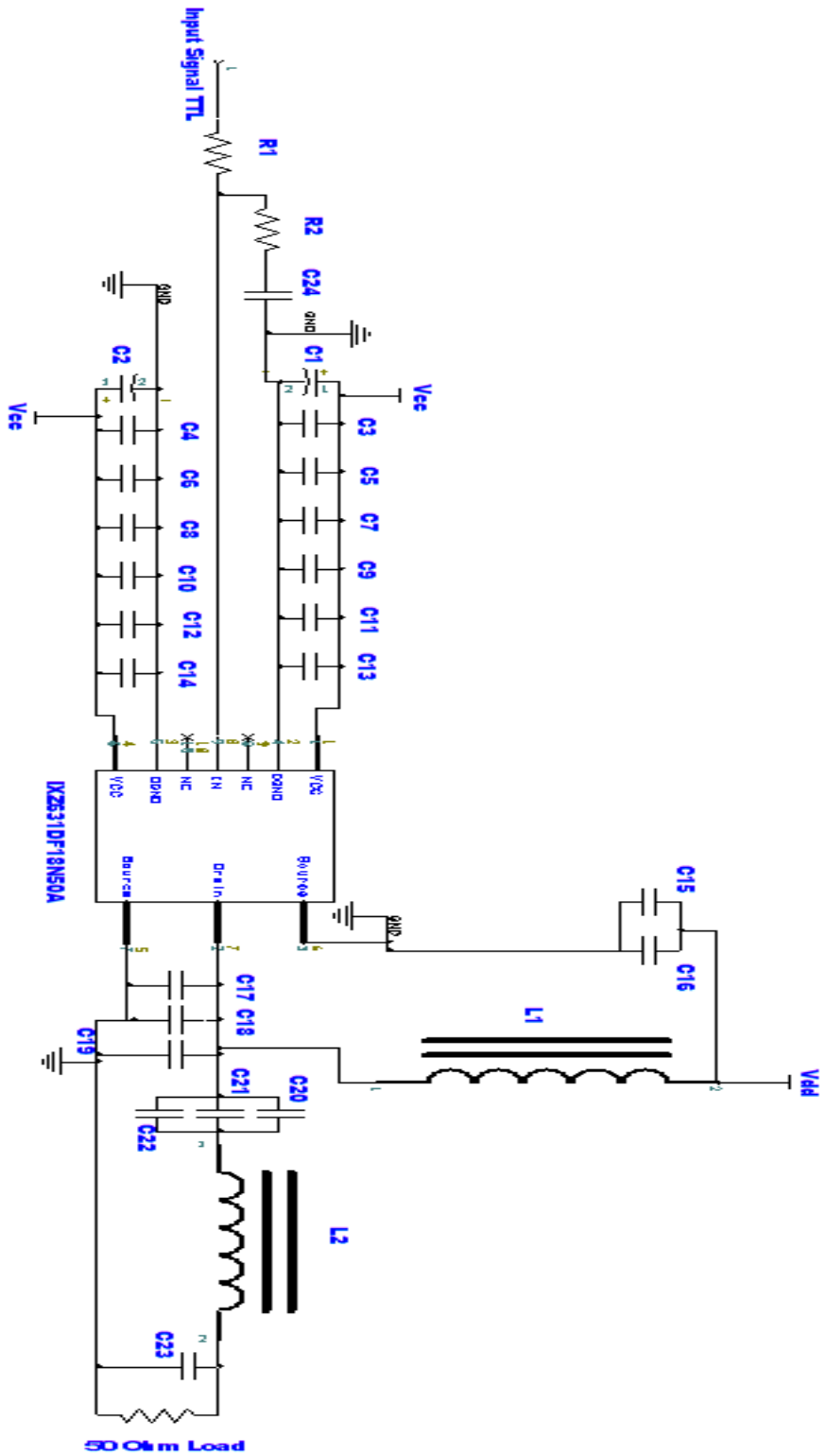


Figure 2 13.56 MHz Schematic



Bill of Materials for 600 W

Item	Qty	Reference	Part	Vendor	Vendor Part #
1	2	C1, C2	4.7 µF 35V Tantalum	Kemet	T491D475K035AT
2	2	C11, C12	0.047 µF 50V	Kemet	C1206C473K5RACTU
3	2	C5, C6	0.01 µF 50V	Kemet	C1206C103K5RACTU
4	2	C3, C4	0.1 µF 50V	Kemet	C1206C104K5RACTU
5	3	C7, C8, C24	0.001 µF	Kemet	C1206C102K5RACTU
6	2	C9, C10	100 pF	Kemet	C1206C101K5RACTU
7	2	C13, C14	0.47 µF	Kemet	C1206C474K5RACTU
8	1	C17	18 pF	ATC	ATC100C180JW2500X
9	1	C18	27 pF	ATC	ATC100C270JW2500X
10	1	C22	33 pF	ATC	ATC100C330JW2500X
11	2	C20, C21	560 pF	ATC	ATC100E561JW2500X
12	1	C19	56 pF	ATC	ATC100C560JW2500X
13	6	C23	430 pF (combination of ATC caps, 10 pF to 100 pF)	ATC	ATC100CXXXJW2500X
15	2	C15, C16	0.1 µF 1000 V	AVX	1825AC104KAZ1A
16	1	L1	400 nH 6 Turns AWG12 on a T200-6		
17	1	L2	10 µH 40 Turns AWG20 on a T106-2		
18	1	R2	1 kΩ	Panasonic	ERJ-8ENF101V
19	1	R1	1 Ω	Panasonic	ERJ-8GEYJ1R0V
20	1	U1	IXZ631DF18N50A	IXYSRF	IXZ631DF18N50
21	1	CONN1	CONN JACK SMB VERTICAL	Tyco Electronics	413990-2
22	1	CONN2	BNC Jack, Right Angle PCB	Tyco Electronics	5413631-1

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Mathew W. Vanis
Directed Energy Inc.