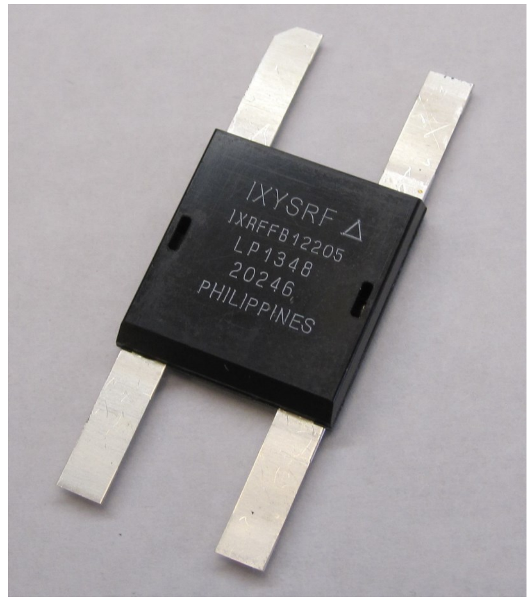
IXRFFB12205 Silicon Carbide Full Wave Bridge Rectifier

1200 V
5 A

Features

- Silicon carbide Schottky diodes
  - No reverse recovery for soft turn-off
  - Temperature independent switching behavior
  - Low leakage current
- Easy to mount, no insulators needed
- High power density
- Isolated substrate
  - High isolation voltage
  - Excellent thermal transfer
  - Increased temperature and power cycling capability
- Very low insertion inductance
- No Beryllium Oxide (BeO) or other hazardous materials
- RoHS compliant



Advantages

- Optimized for high speed
- Easy to mount, no insulators needed
- High power density

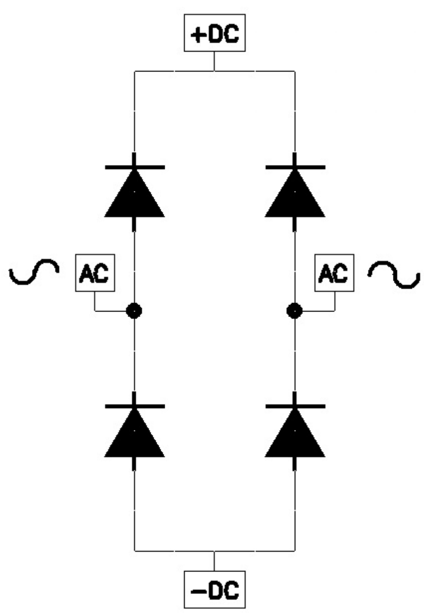
Applications

- Output rectifier for high frequency power converters
- General high speed rectifier circuits

Description

The IXRFFB12205 is a 1200 V, 5 A silicon carbide diode full bridge rectifier packaged in IXYSRFs low-inductance RF package incorporating layout techniques to minimize stray lead inductances for optimum performance. The benefits of silicon carbide include faster operation due to the minimal reverse recovery from only the stored charge of the junction capacitance. The IXRFFB12205 takes advantage of silicon carbide's high surge current capability, and is mounted in our RF package, to provide exceptional thermal resistance properties that enhance high frequency operation. It is a surface-mountable device.

Figure 1 Functional diagram



Device Specifications

Symbol	Parameter	Test Conditions	Maximum Ratings	
V_{RRM}	Repetitive peak reverse voltage		1200	V
V_{RSM}	Repetitive surge reverse voltage		1200	V
V_{DC}	DC blocking voltage		1200	V
$I_{F(AVG)}$	Average forward current (per diode)	T_J = 175°C	5	A
I_{FRM}	Repetitive peak forward surge current (per diode)	T_C = 25°C, t_P = 10 ms Half sine wave	30	A
I_{FSM}	Non-repetitive peak forward surge current (per diode)	T_C = 25°C, t_P = 10 µs Pulse	100	A
T_{OT}	Operating temperature		- 40°C to 85°C	°C
T_{VJ}	Operating virtual junction temperature		- 55 to +175	°C
T_{STG}	Storage temperature		- 55 to +175	°C
P_{TOT}	Power total	T_C = 25 °C (37.5 W per diode)	150	W

Device Performance

Symbol	Parameter	Test Conditions	Characteristic Values		
T_J = 25°C unless otherwise specified **Note 1**			Typ.	Max.	Units
V_F	Forward voltage	I_F = 5 A, T_J = 25°C T_J = 175°C	1.6 3.6	1.8 3.8	V
I_R	Reverse current	V_R = 1200 V, T_J = 25°C T_J = 175°C	10 20	50 200	µA
C_J	Junction capacitance	f = 1 MHz, V_R = 0 V V_R = 500 V V_R = 1000 V	450 75 65		pF
R_{THJC}	Thermal resistance		1		°C/W
T_L	Lead soldering temperature	1.6 mm (0.063 in) from case for 10 s	300		°C
Isolation	Pin to substrate Pin to pin		>1800 >1500		V_{RMS}
C_{stray}	Stray capacitance	f = 1 MHz Any one pin to the metallized back	46		pF
Weight			2		g

Note: All performance characteristics are per diode in bridge

Note: All charts are per diode in bridge

Fig. 2

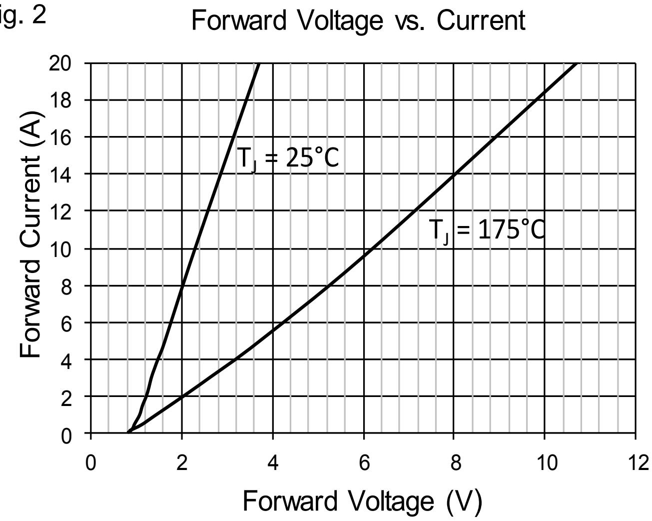


Fig. 3

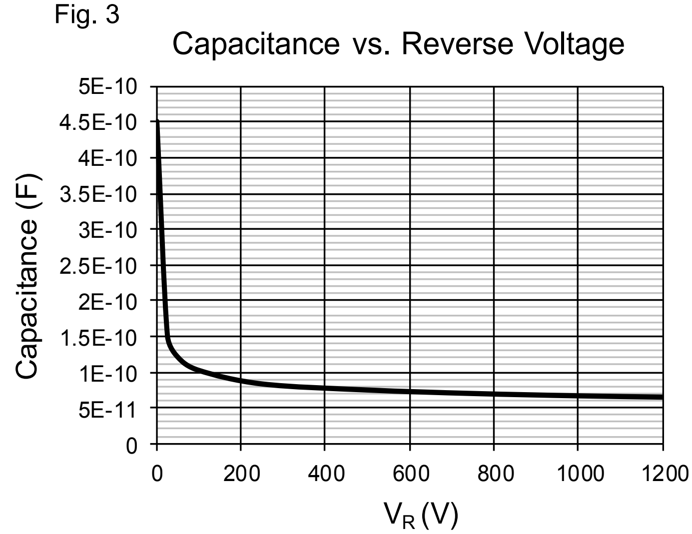


Fig. 4

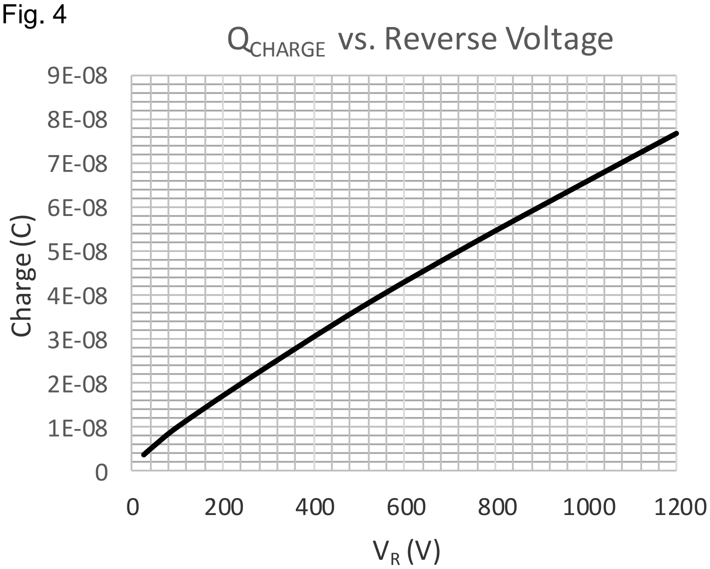


Fig. 5

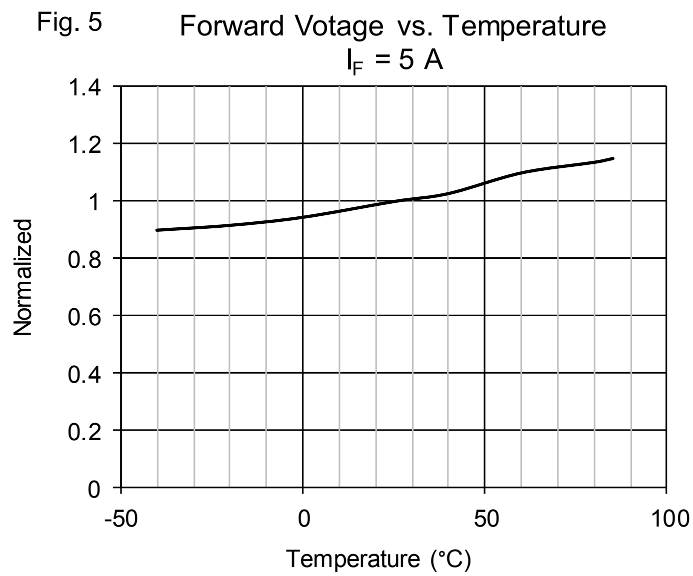


Fig. 6

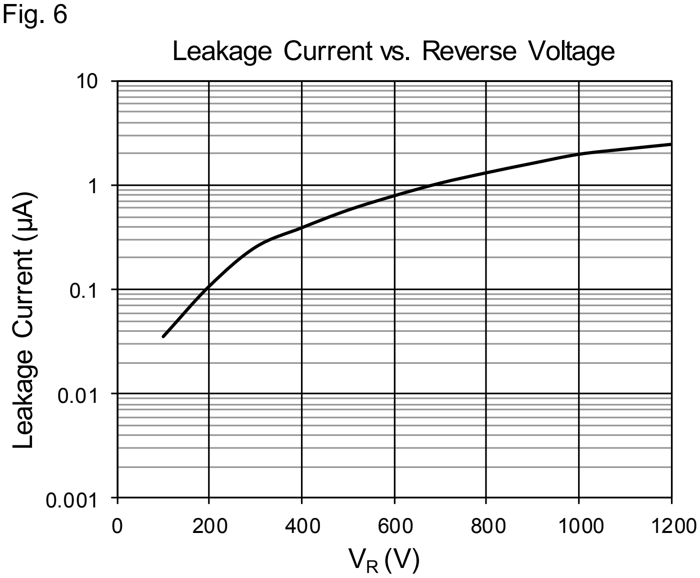
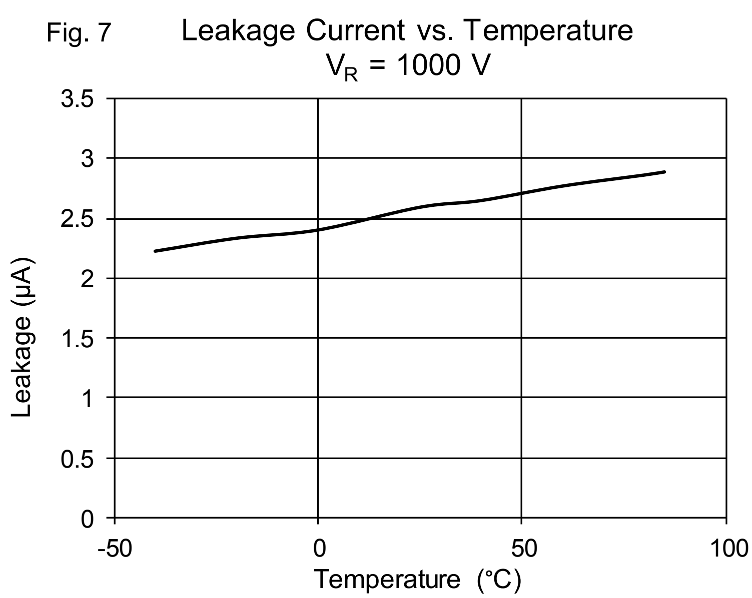


Fig. 7



Lead description

SYMBOL	FUNCTION	DESCRIPTION
+ DC	Positive DC	Positive DC output of bridge rectifier
- DC	Negative DC	Negative DC output of bridge rectifier
AC IN	AC input	AC input to bridge rectifier
AC IN	AC input	AC input to bridge rectifier

Figure 8 Package drawing

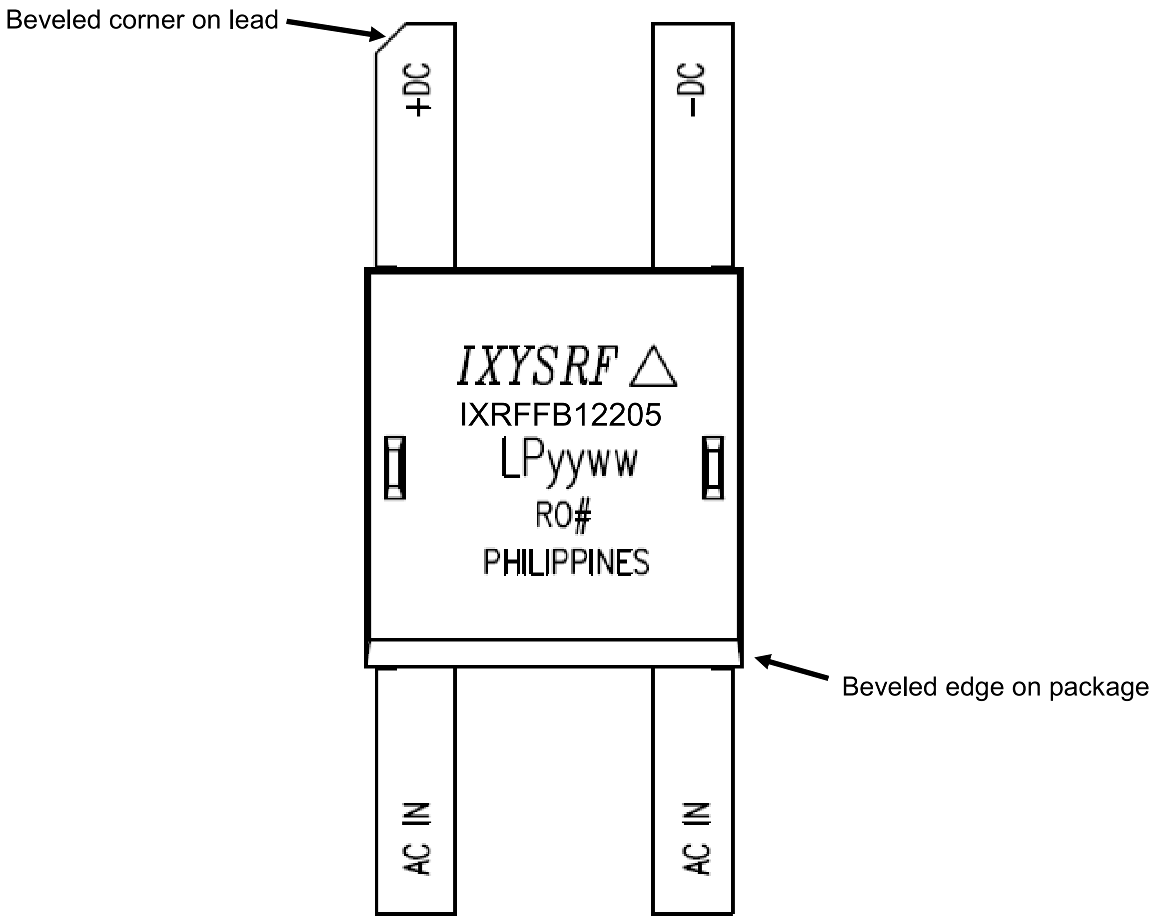
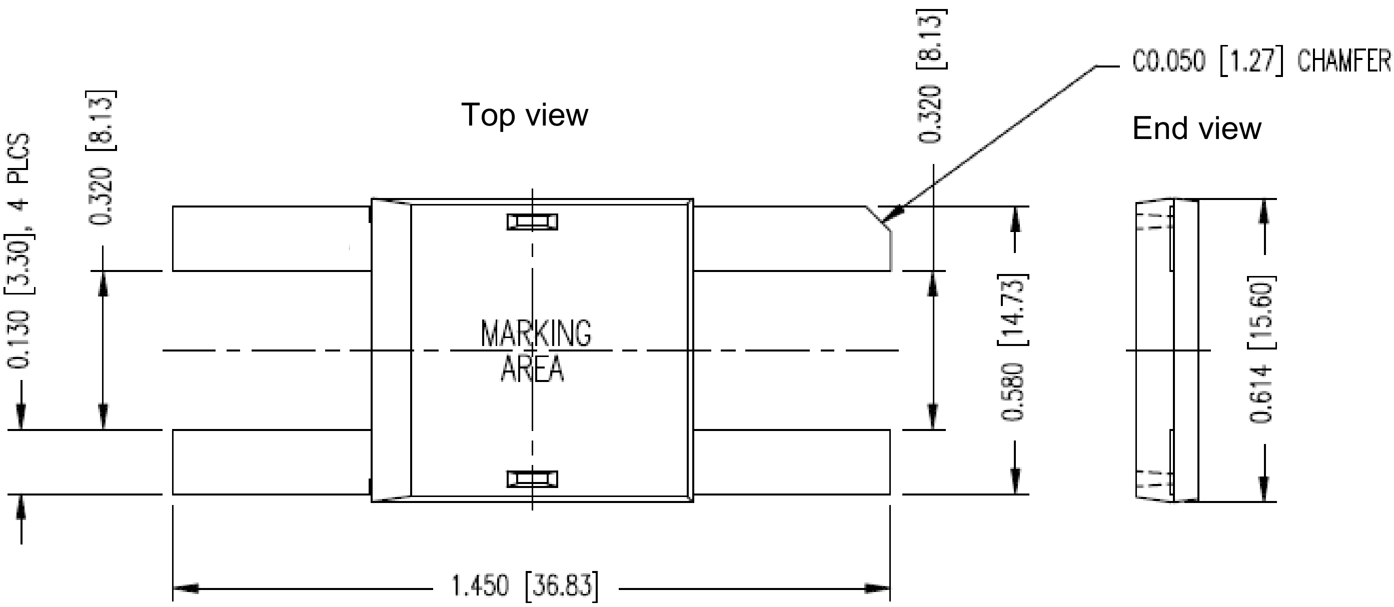
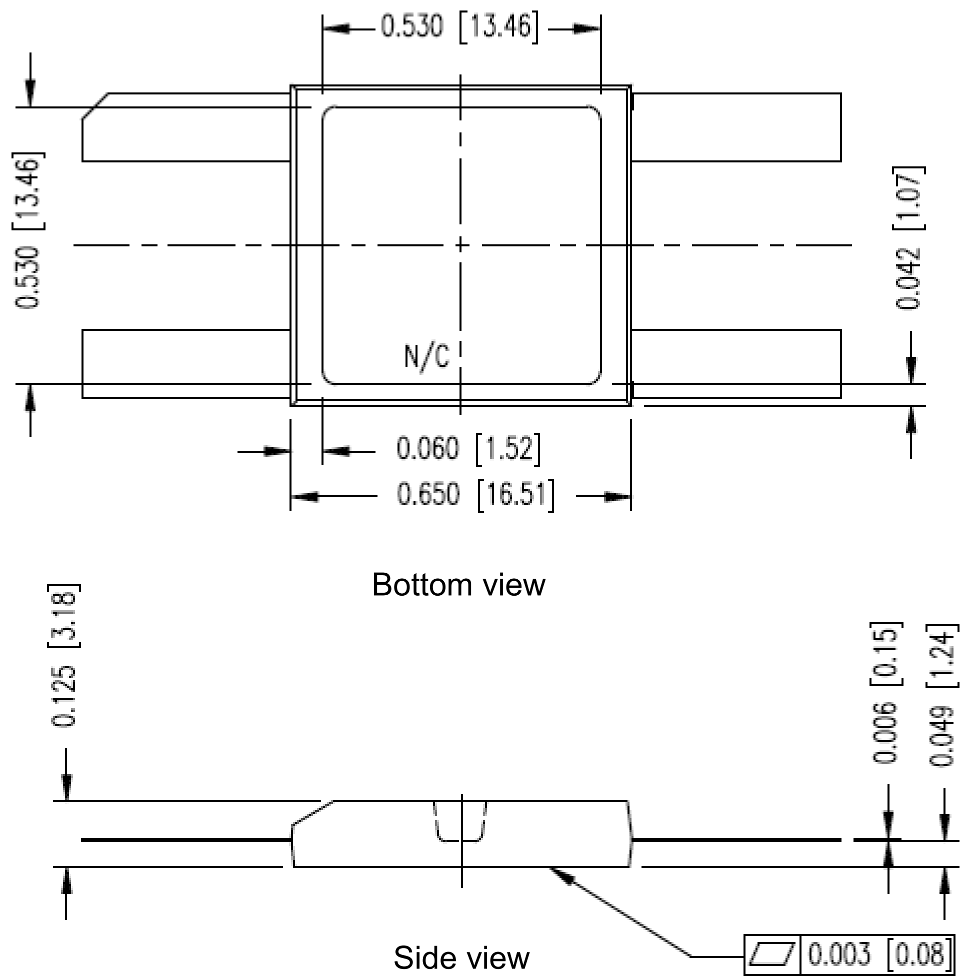


Figure 9 IXRFFB12205 package dimensions





IXYSRF reserves the right to change limits, test conditions, and dimensions without notice.

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Frequency estimations

The maximum frequency is estimated indirectly through the power dissipation Pd of the device, which is a combination of conduction and switching losses.

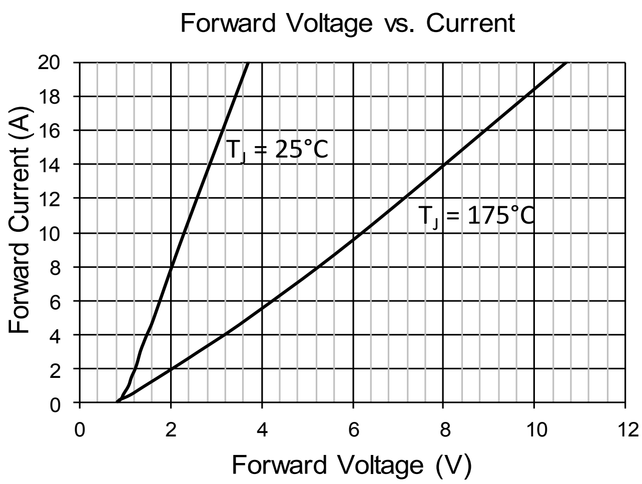
$P_d = P_{cond} + P_{switching}$

Conduction losses P_{cond}

Two steps are performed to determine the P_{cond} conduction losses:

Step 1, map out forward voltage versus current in an oven at 175° C, which is the maximum die temperature. These values are plotted in the chart below for a single diode.

Step 2, apply DC current until the forward voltage matches the value at 175° C while maintaining a 25° C case temperature. During testing it was determined that 156 W of forward power was needed to reach the forward voltage found in step 1 above. A rounded value of 150 W is used for calculations and was entered on this datasheet for parameter P_{TOT}.



Expressing P_{cond}

$$P_{cond}(T_J) = V_{TO}(T_J) * I_{F(AVG)} + R_D(T_J) * I^2_{F(RMS)}$$

On the above chart, the forward voltage and current characteristics, V_F and I_F, can be approximated by a straight line defined by the threshold voltage V_{TO} and the dynamic resistance R_D. These quantities are determined from the chart for two forward current levels I_{F1} and I_{F2} at a given junction temperature T_J and are used in the P_{cond} calculations.

$$V_F(I_{F1}, T_J) = V_{TO}(T_J) + R_D(T_J) * I_{F1}$$

$$V_F(I_{F2}, T_J) = V_{TO}(T_J) + R_D(T_J) * I_{F2}$$

Derive the below expressions using the above equations:

$$R_D(T_J) = \frac{V_F(I_{F2}, T_J) - V_F(I_{F1}, T_J)}{I_{F2} - I_{F1}}$$

$$V_{TO}(T_J) = \frac{V_F(I_{F1}, T_J)*I_{F2} - V_F(I_{F2}, T_J)*I_{F1}}{I_{F2} - I_{F1}}$$

For convenience in determining $I_{F(AVG)}$ and $I_{F(RMS)}$, a sinusoidal waveform is applied for rectification through the full-wave bridge. We can write the following equations for a rectified sine-wave, where I_{MAX} is the rated current of the device at the maximum junction temperature. The duty-cycle d = 1 for a full-wave bridge meaning that the bridge is conducting for the full period of the input signal.

Formulas for the average and RMS full-wave current:

$$I_{F(AVG)} = \frac{2\,I_{MAX}}{\pi} * d \qquad I_{F(RMS)} = I_{MAX} * \sqrt{\frac{d}{2}}$$

For d = 1

$$I_{F(AVG)} = \frac{2\,I_{MAX}}{\pi} \qquad I_{F(RMS)} = \frac{I_{MAX}}{\sqrt{2}}$$

Resulting average and RMS values when calculated with the rated current of 5 A at maximum temperature

Part number	I_{MAX} (A)	$I_{F(AVG)}$ (A)	$I_{F(RMS)}$ (A)
IXRFFB12205	5	3.18	3.54

R_D and V_{TO} values where V_1, I_1, and V_2, I_2 are points along the 175° C plot

Part number	I_2 (A)	I_1(A)	V_2(V)	V_1 (V)	R_D (Ω)	V_{TO} (V)
IXRFFB12205	5	2	3.6	2	0.53	0.93

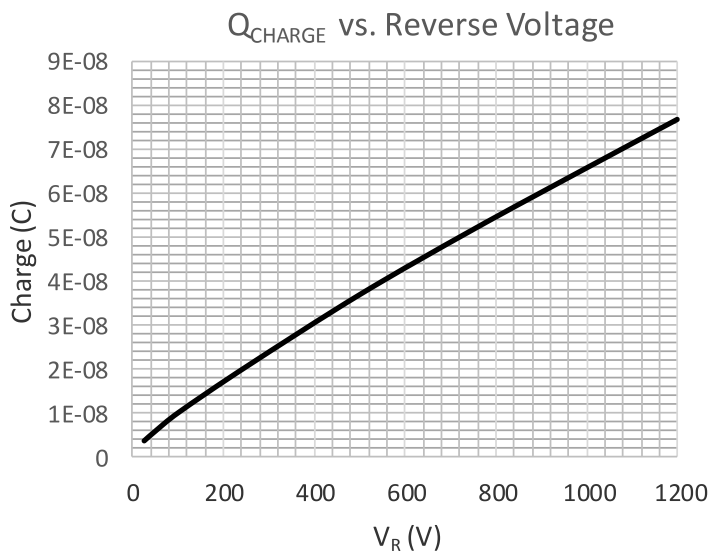
Conduction losses are now calculated- $P_{cond}(T_J) = V_{TO}(T_J) * I_{F(AVG)} + R_D(T_J) * I^2_{F(RMS)}$

Part number	P_{cond} (W) full wave
IXRFFB12205	9.6

Switching losses $P_{switching}$

$P_{switching}$ = Qc * Vo * Fs   where Qc is the capacitive charge in nanocoulombs, Vo is the output voltage, and Fs is the switching frequency.

The following chart represents the total capacitive charge, Qc, of the bridge with two series strings in parallel that results in a total charge calculated as a single diode.



Power available for switching $P_{switching} = P_d - P_{cond}$

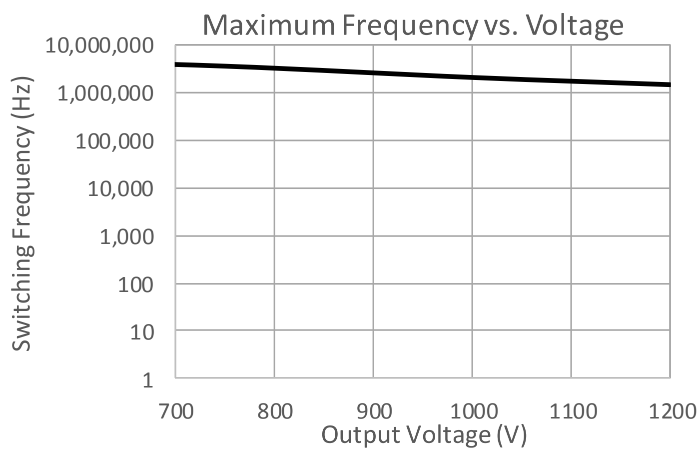
Part number	Pd	P_{cond} (W) full wave	$P_{switching}$ (W) full wave
IXRFFB12205	150	9.6	140.4

Switching frequencies

$P_{switching}$ = Qc * Vo * Fs   or Fs = ($P_{switching}$) /(Qc * Vo)

Part number	$P_{switching}$ (W) full wave	Vo (V)	Q_C (nC)	Fs (Hz)
IXRFFB12205	140.4	700	50	4011428
		1200	77	1519480

In using the maximum heat capacity of the package with the four diodes in the bridge configuration, the calculated switching frequency can range greater than 4 MHz depending on the operating voltage.



The above chart plots potential switching frequencies for the IXRFFB12205 when utilizing all four diodes to heat the device package until the 175°C maximum die temperature is reached while maintaining a 25°C case temperature. Derating for higher case temperatures is calculated by using the standard power formula to find the new power limit.

$$\text{Power capacity (W)} = \frac{\text{Max die temp (°C)} - \text{Case temp (°C)}}{\text{Thermal resistance of package } (\frac{°C}{W})} = \frac{175\ °C - \text{Case temp } °C}{1\ \frac{°C}{W}}$$

If it is not possible to maintain a case temperature of 25° C, a new power limit can be calculated and a new frequency limitation determined.

From the pure calculation sense the smaller the stored charge and lower operating voltage, the higher the switching frequency. However, when used at high frequencies the parasitic components will impact operation. Inductance of the device package and circuit board must be considered in the final design to achieve optimum operation. It is important to make circuit board layouts as compact as possible to minimize the impact of the parasitic inductance. The junction capacitance also impacts high frequency operation as the junction impedance loads the circuit, resulting in a reduce rectified voltage. In a practical application, best operation is achieved when frequency of operation is below 8 MHz.