The destructive effects of Kelvin leaded packages in high speed, high frequency operation

Directed Energy, Inc. • 2401 Research Blvd., Ste 108 • Fort Collins, CO 80526
TEL: 970-493-1901 • FAX: 970-493-1903 • EMAIIL: deiinfo@directedenergy.com • WEB: www.directedenergy.com

ABSTRACT

Today power MOSFET die technology is not the only limiting factor in achieving the high switching speeds and higher frequencies targeted as goals by the RF and HF power communities. The choice of package is often the fundamental cause of most of the problems found when attempting to operate power MOSFETs at high switching speeds and high frequencies. These problems can appear as unstable operation in the most benign conditions and as unexplained failure and radically reduced reliability in the worst cases. This paper will explore in detail the impact of intermediate speed enhancement techniques, such as the Kelvin lead, without commensurate attention to other stray inductive terms.

Introduction

MOSFET die is inherently a high speed device The theoretical switching speed of well designed die is on the order of 200ps (200E-12S). There are, of course, many die designs which are far from optimum. But for this article we will assume a near optimum die design. This brings us to the package and its inherent stray inductive terms.

The traditional TO-3 and TO-247 packages were not designed with high frequency operation in mind. In fact, the TO-3 that originated in the late 1950s mimics the octal pin pattern of a vacuum tube. Little or no consideration was given to high frequency, inductance, or thermally induced stress issues.

Plastic TO-220 and TO 247 packages followed, providing some improvement over the TO-3. They are smaller and capable of slightly improved switching speeds but are not hermetic packages.

The TO-3 package still dominates in high reliability applications such as military avionics. New packaging approaches, such is the TO-218 and the TO-254, and large "block" configurations have appeared. However, they are not well-suited to high frequency operation because they have, among other shortcomings, highly inductive topologies.

Figure 1 shows the outlines of some of these devices. Most have invoked a Kelvin lead for switching speed enhancement. This technique, when used without equal refinements in packaging design with regard to other stray inductive terms, can be disastrous.

Figure 2 illustrates the MOSFET model most often used not only for circuit design but by manufacturers to describe device operation and performance as well. When switching speeds approach 20ns (20E-9S) or lower and the frequency approaches 1MHz (1E6Hz) and above, this model is completely inadequate. It is interesting to note that the model in Figure 2 is used not only for circuit design, but also for discussion of dv/dt phenomenon and avalanche breakdown. Both effects occur at speeds well above the model's ability to predict results.

Figure 3 is a model more appropriate to both circuit design and device performance characterization at high speeds and high frequency operation. Using this model and a high speed differential measurement test fixture, a variety of devices were studied. The balance of this report will deal with the results of that study. (1)

V_{LS} and V_{LD} During Turn-Off

Referring to Figure 3, when we apply a +15V input to the gate terminal of the device, it commutates as shown by the current I_{DS} in the scope photo of the waveforms in Figure 4. However this rising current in the source lead inductance L_S produces a negative feedback term V_{LS} which limits the rate of current rise in the source (dI_D/dt). Here we see a V_{LS} term of 28V produced by a 32A current pulse measured in a TO-3 package. In this system the source lead inductance is a di/dt limiter such that for most circuit configurations, the V_{LS} term stays below 30V. However, with sufficiently poor layout in either package design or circuit design, this may not be the case. For standard three leaded pack-

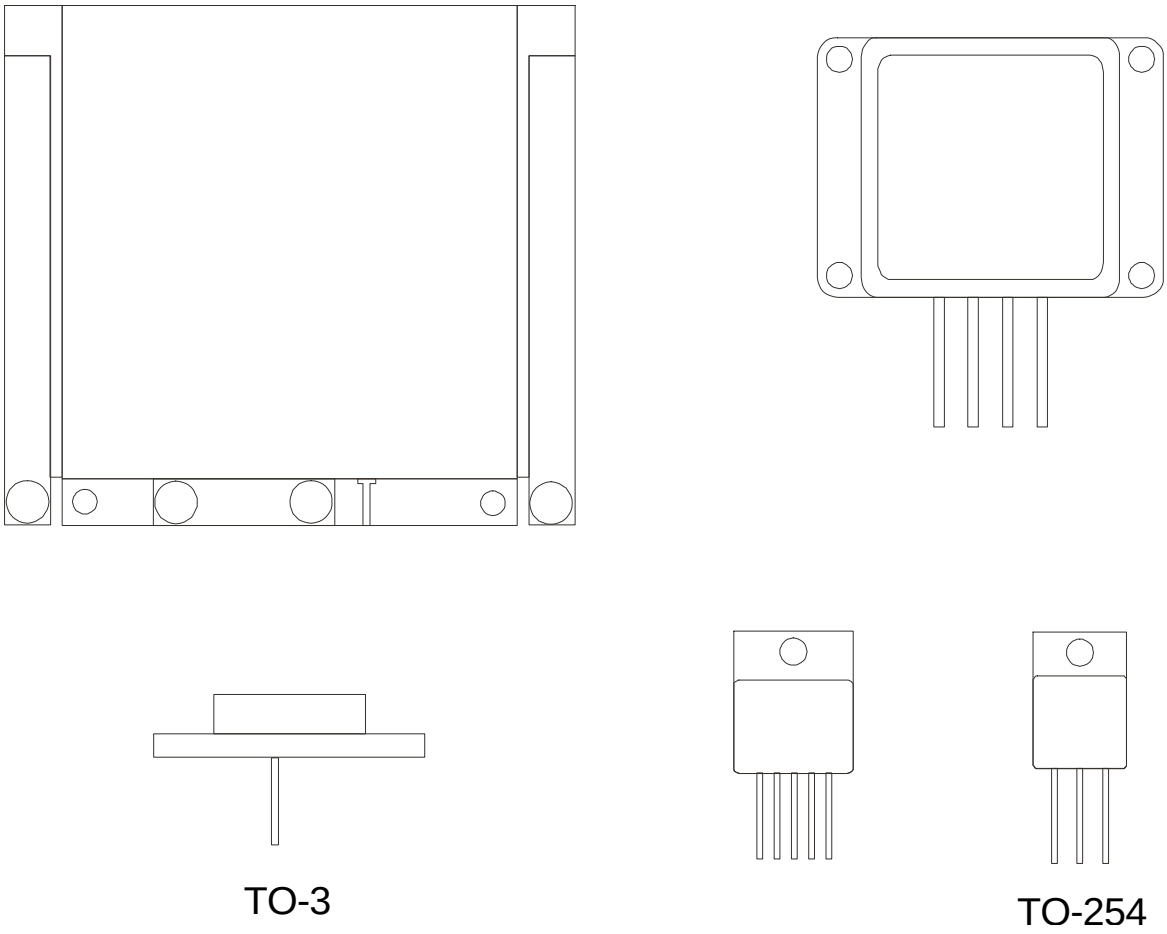

FIGURE 1. Conventional package outlines (all packages shown approximately actual size).

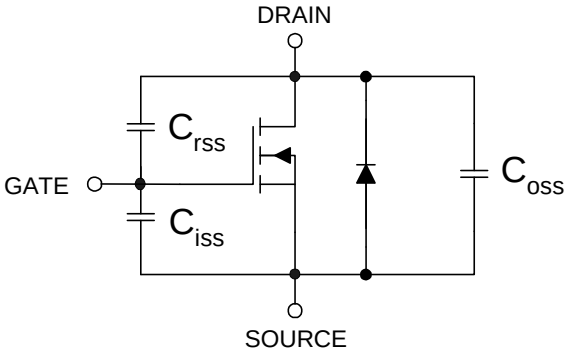

FIGURE 2. Standard MOSFET model.

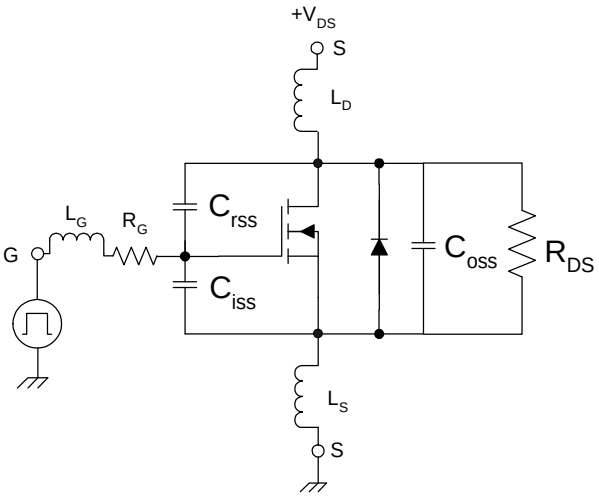

FIGURE 3. Complete MOSFET model.

ages, this negative feedback term is the primary cause for poor speed performance. Attempting to eliminate the effects of this negative feedback, a Kelvin lead has been installed in some packages, as was shown in Figure 1.

Figure 5 is a model of a typical Kelvin lead package. When this package design is invoked, there are several assumptions made, one of which is that the negative terminal of the gate drive will track the top of L_S as the current rises. However, we also have an inductor L_{SK} and C_S as a series and shunt element preventing the negative terminal

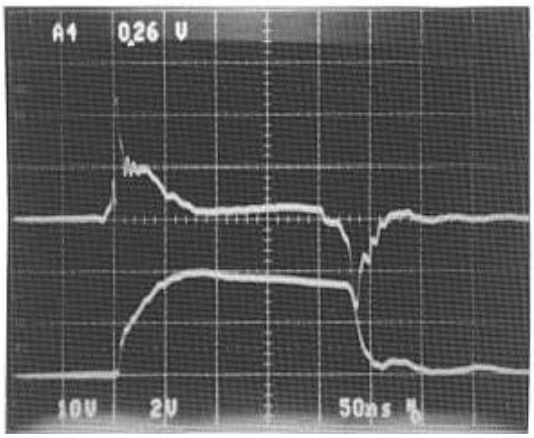

FIGURE 4. V_{LS} and I_{DS} waveforms.

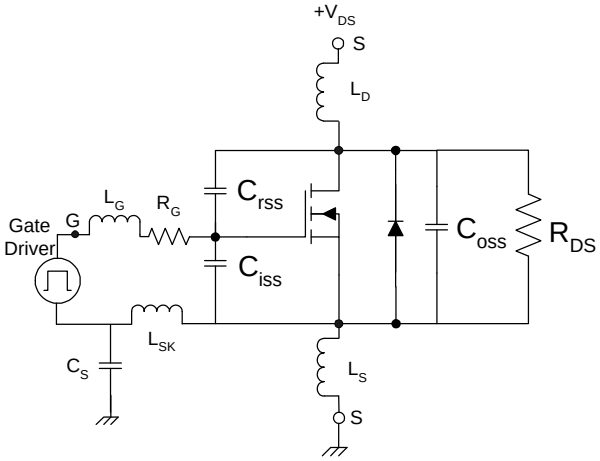

FIGURE 5. Kelvin lead MOSFET Model.

from really following the L_S di/dt term very closely. The Kelvin lead does eliminate much of the negative feedback and provides a faster current rise, as shown in Figure 6B and the top photo. Also notice that the magnitude of the L_S di/dt term in Figure 6 and the top photo is now 50V.

From Figures 6A, 6B and the adjacent photo

V_{LS} = 50V

di = 32A

dt = 10 x 10E-9

Then

$L_S = V_{LS}$di/dt = 15nH (15E-9H)

In packages like those illustrated in Figure 1, L_S can easily be 30nH (30E-9H)or larger. Furthermore, in these package styles L_D can approach an equally large number. If we use the peak current ratings of some of the larger of these devices, V_{LD} can become a problem.

$V_{LD} = L_D$ di/dt

L_D = 30nH (30E-9H)

di = 100A

dt = 10nS (10E-9S)

Then

V_{LD} = (30 x 10E-9)(100/10 x 10E-9) = 300V

If we look at the V_{LD} term in Figure 6C and the V_{LS} term in Figure 6D in the timing chart, we see that the V_{LD} and V_{LS} terms subtract from the external V_{DS} term during turn-on at t_0. But during turn-off they add to the external V_{DS} term. Therefore given devices as illustrated in Figure 1, it is very easy in a high power high speed circuit, to have a net 600V transient during turn-off which is resident inside the package and totally transparent to the user. This turn-off transient analysis could explain phantom failures attributed to high speed high power MOSFET circuits.

In addition to the V_{LS} and V_{LD} terms during turn-off, there is an additional problem. Figure 6E also shows the V_{LSK} term across the Kelvin source lead inductance. At this point in time the gate of the device is at 0V, as shown in Figure 6A, while the source node is at -V>4V which will turn the device back on as illustrated by the waveform in Figure 6F and the bottom photo. This dampened oscillation is caused by the gate Kelvin tank circuit comprised of L_G, L_{SK},R_G, C_{iss} and the L_{GD}, R_{GD}, and C_{GD} terms of the gate driver. This oscillation can be exacerbated by C_{rss} and the Miller Effect.

If by poor circuit layout, we increase the value of L_S, or with even higher peak currents than those illustrated, the L_{SK}, L_S gate ring can cause a string of current pulses in the drain of descending amplitude as shown in Figure 6G. The effects of larger external L_S predominately provide a larger driving L di/dt term for the gate Kelvin tank in which larger currents increases the effect of both internal and external inductive terms. In a high frequency power converter this type of spurious behavior could cause erratic operation and increased EMI if not cross conduction failures.

In the center photo of Figure 6, we see a high frequency oscillation on the V_{LSK} term, illustrated in Figure 6E. This is the C_S, L_{SK} and L_S tank circuit. Its resonant frequency is much higher than the gate tank circuit, and it is easily dampened by stray resistance. However, in linear applications this oscillation could also lead to stability and or linearity problems.

DE-SERIES MOSFET Devices

Shown in Figure 7 are the four families of the DE-SERIES power MOSFET. This device was designed from the onset with high voltage, high speed and high power as the driving guidelines. (2) Figure 8 shows the V_{LS} and the I_{DS} for the DE-275, with test conditions as follows. From Figure 8, we see that:

V_{Ls} = 8V

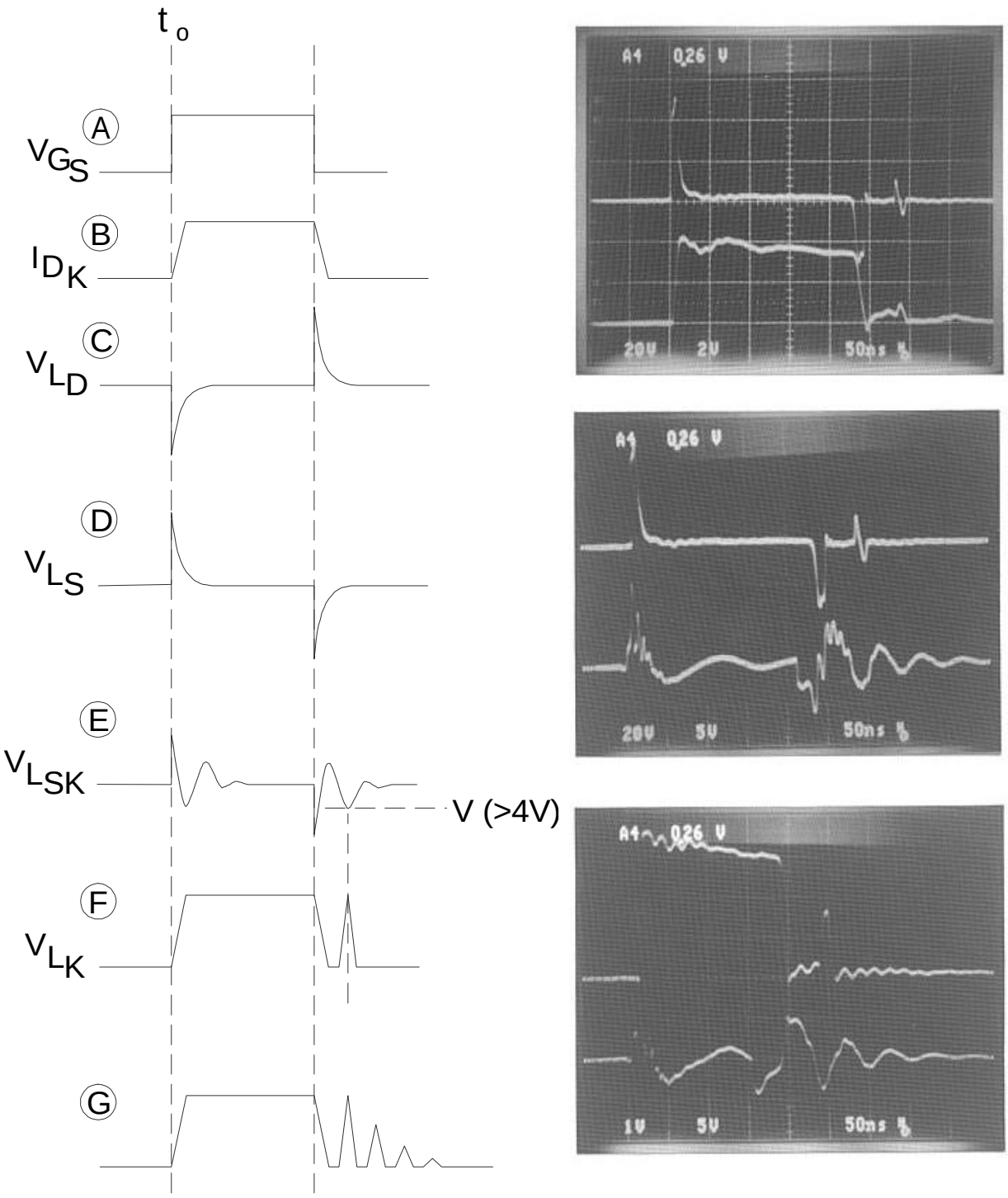

FIGURE 6. Timing chart of model waveforms and data.

di = 32A
dt = 8 x 10E-9S

Using these values

$L_S = V_{Ls}\ dt/di = 2nH$ (2E-9H)

In these devices $L_D \leq 1nH$ (1E-9H) so that total insertion inductance is ≤ 3nH (3E-9H). Comparing this value to the ≥30nH (30E-9H) value for more conventional devices, we see a full order of magnitude in reduced inductance.

These lower values of L_S and L_D greatly reduce, if not eliminate, the effects of both the gate Kelvin tank oscillation and the V_{DS} over-voltage

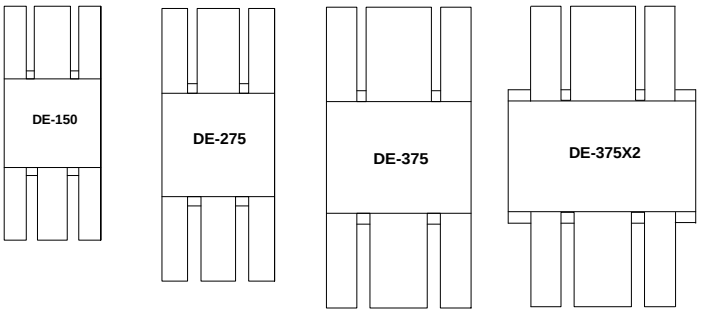

FIGURE 7. DEI DE Series high speed, high frequency power MOSFETs (all packages approximately actual size).

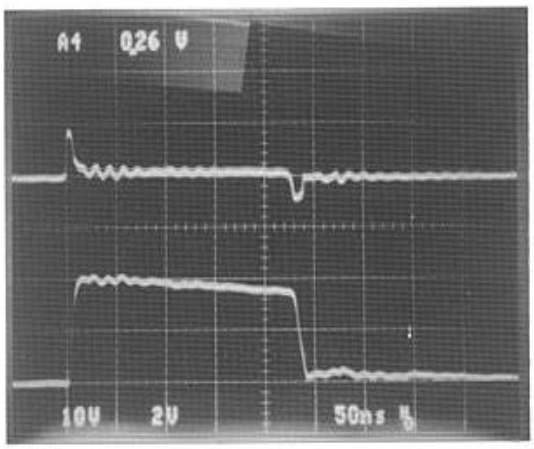

FIGURE 8. DE-275 L_S di/dt term (top) and current waveform (bottom).

spike during turn-off. As stated earlier, both of these conditions can lead to erratic behavior, increased EMI, and cross-conduction failures.

Conclusion

With their low thermal impedance, low inductance, symmetric surface-mount design and fast switching speed, the DE-Series MOSFETs are clearly the transistor of choice for high speed power circuits. Their design reduces the values of L_S and L_D by an order of magnitude over competing power MOSFET devices.

However the circuit designer must be keenly aware that having the correct high-speed device is only part of the solution. Circuit topology and layout as well as selecting the correct passive components all play significant roles in good high-speed circuit design. The circuit analysis must include all strays, both L, R and C from the power source to the load. We have shown that failure to take all these terms in account can lead to not only poor package and circuit designs, but device and system failure as well.

References

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DE-SERIES Fast Power MOSFET – An Introduction